GWM60S50

POWER FIELD EFFECT TRANSISTOR

GENERAL DESCRIPTION

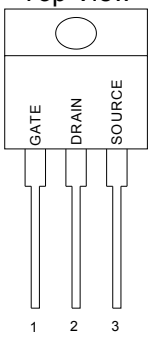
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

FEATURES

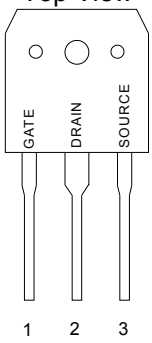
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and V_{DS}(on) Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware

PIN CONFIGURATION

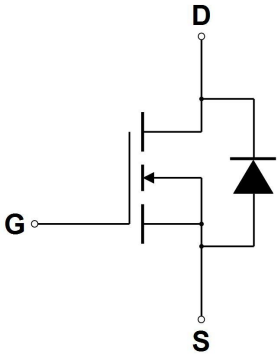
TO-220F
Top View



TO-3P/TO-247
Top View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	$I_{D\ (1)}$	60.2	A
— Pulsed	I_{DM}	180.6	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
Total Power Dissipation – TO-220FP	P_D	54	W
–TO-3P		500	
–TO-247		379	
Derate above 25℃ – TO-220FP		0.43	W/℃
–TO-3P		4.0	
–TO-247		3.03	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Single Pulse Drain-to-Source Avalanche Energy — T_J = 25℃ (V_{DD} = 100V, V_{GS} = 10V, I_L = 16A, L = 10mH, R_G = 25Ω)	E_{AS}	1280	mJ
Thermal Resistance — Junction to Case -TO-220FP	θ_{JC}	2.3	℃/W
— Junction to Case -TO-3P		0.25	
— Junction to Case -TO-247		0.33	
— Junction to Ambient -TO-220FP	θ_{JA}	62.5	
— Junction to Ambient -TO-3P ,TO-247		40	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	℃

(1) Drain current limited by maximum junction temperature

ORDERING INFORMATION

Part Number	TOP MARK	Part Number	Packing Mthod	Note
GWM60S50XN220FP (Notte1)	GWM60S50X	TO-220FP	Tube	
GWM60S50XN3P (Notte1)	GWM60S50X	TO-3P	Tube	
GWM60S50XN247 (Notte1)	GWM60S50X	TO-247	Tube	

Note1: X : Suffix for Halogen Free Product,

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25℃.

			GWM60S50			
Characteristic		**Symbol**	**Min**	**Typ**	**Max**	**Units**
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μA)		$V_{(BR)DSS}$	500			V
Drain-Source Leakage Current (V_{DS} =500 V, V_{GS} = 0 V)		I_{DSS}			1	uA
Gate-Source Leakage Current-Forward (V_{gsf} = 20 V, V_{DS} = 0 V)		I_{GSSF}			100	nA
Gate-Source Leakage Current-Reverse (V_{gsr} = - 20 V, V_{DS} = 0 V)		I_{GSSR}			100	nA
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2	3	4	V
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 20A) *		$R_{DS(on)}$			56	mΩ
Gate resistance (f=1MHz, open drain)		R_G		3.9		Ω
Input Capacitance	(V_{DS} = 100 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}		2973		pF
Output Capacitance		C_{oss}		68		pF
Reverse Transfer Capacitance		C_{rss}		51		pF
Turn-On Delay Time	(V_{DD} = 250 V, I_D = 60 A, R_G = 25Ω) *	$t_{d(on)}$		51.3		ns
Rise Time		t_r		147.3		ns
Turn-Off Delay Time		$t_{d(off)}$		126.7		ns
Fall Time		t_f		74.8		ns
Total Gate Charge	(V_{DS} = 400 V, I_D = 60 A, V_{GS} = 10 V)*	Q_g		66.2		nC
Gate-Source Charge		Q_{gs}		23.6		nC
Gate-Drain Charge		Q_{gd}		27.5		nC
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage(1)	(I_S = 60 A, d_{IS}/d_t = 100A/μs)	V_{SD}			1.5	V
Forward Turn-On Time		t_{on}		**		ns
Reverse Recovery Time		t_{rr}		503.46		ns

* Pulse Test: Pulse Width ≦300μs, Duty Cycle ≦2%

** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS

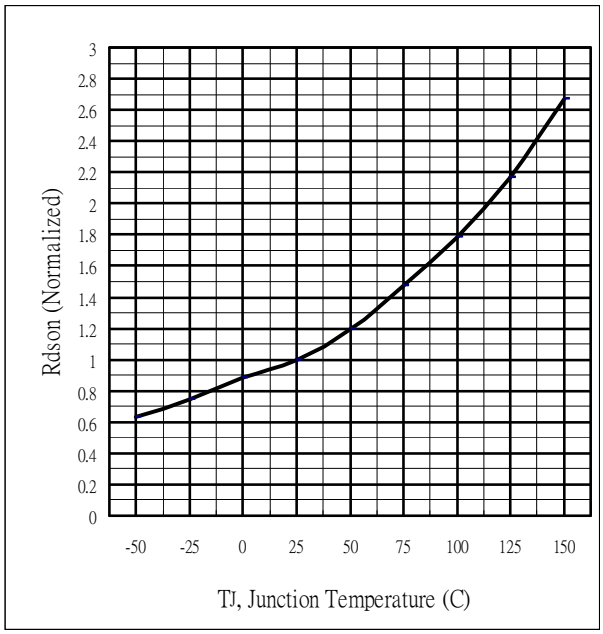


Fig 1. On-Resistance Variation with vs. Temperature

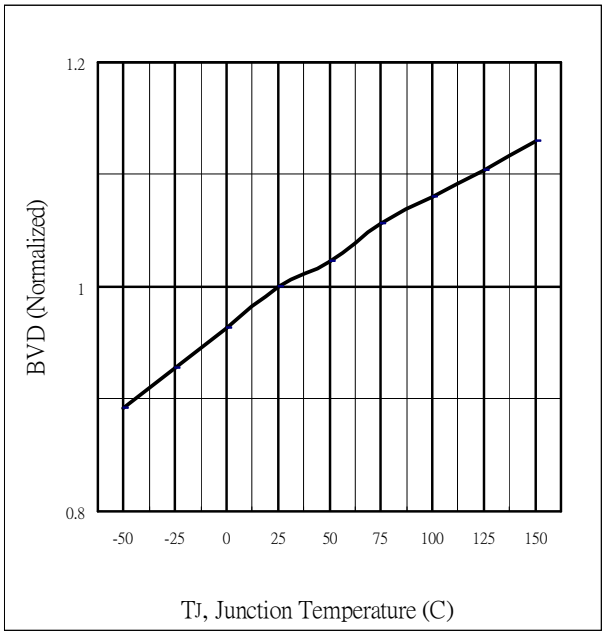


Fig.2 Breakdown Voltage Variation vs. Temperature

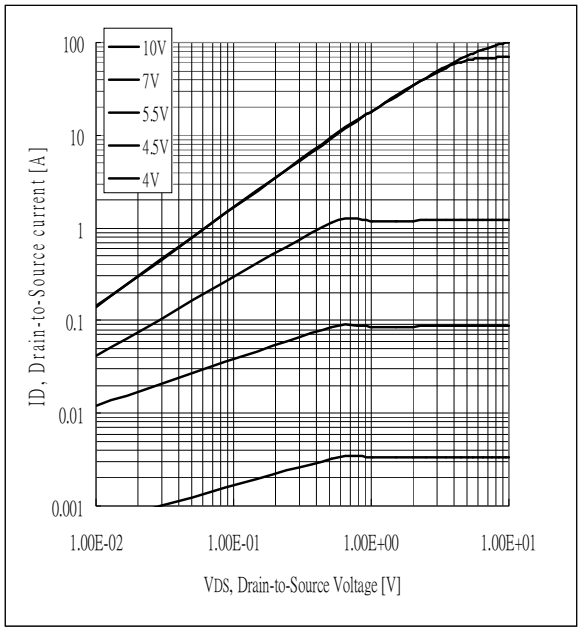


Fig 3. Typical Output Characteristics

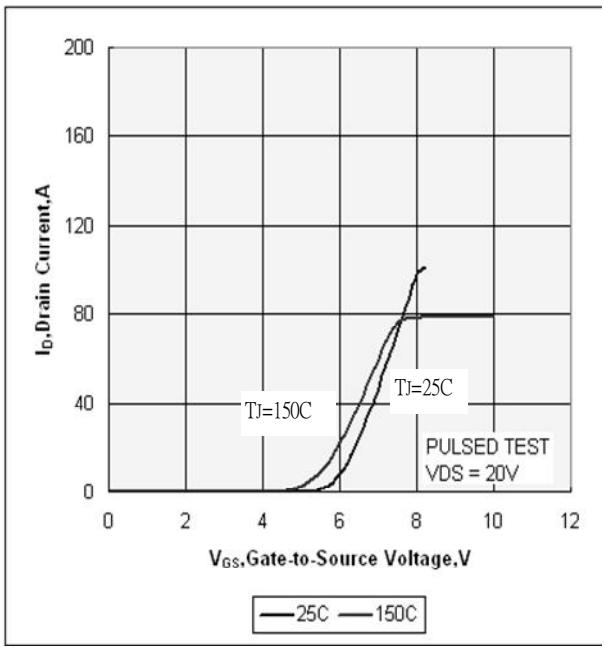


Fig 4. Typical Transfer Characteristics

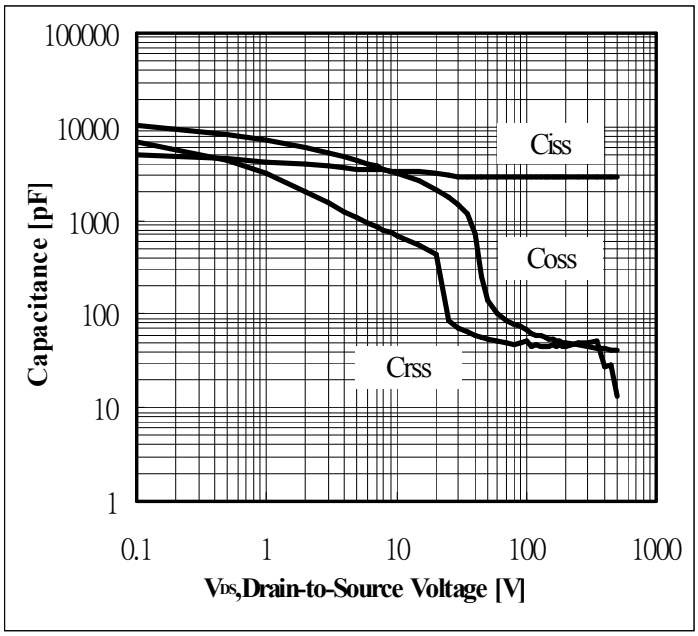


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

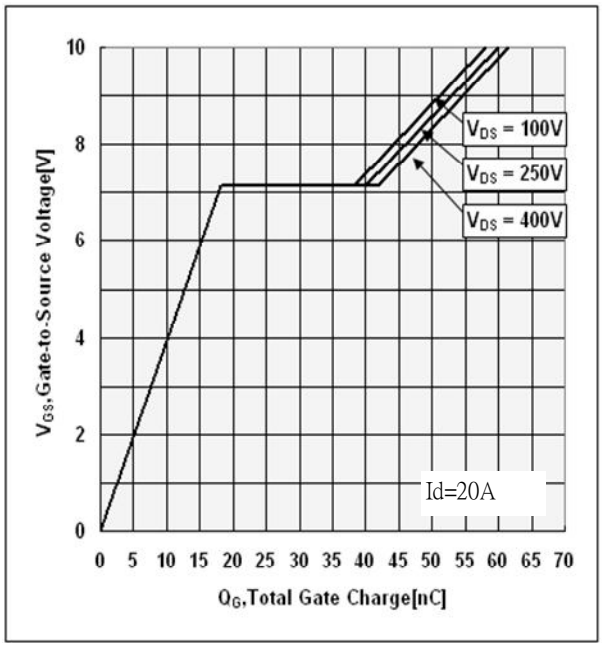


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage